FACULTY PROFILE

Name of Teaching Staff / RMK ID	**Dr.S.KARUNAKARAN / T1211**		
Designation	Associate Professor (Gr-II)		
Department	Electronics Engineering (VLSI Design and Technology)		
Date of Joining the Institution	21.11.2025		
Qualifications	B.E (EEE)	M.E (VLSI Design)	Ph.D (VLSI Design)
Total Experience	Overall : 20 Years 1 month	in RMK : 1 Month	
Papers Published in Journal	Overall : 25	After Joining RMK :	
List of Papers Published	1.Chandan Choubey,M. Dhanalakshmi, **S.Karunakaran**, Gaurav Vishnu Londhe,Vrince Vimal,M. K. Kirubakaran "Optimizing Bio-Imaging: Quantum Computing Inspired Bald Eagle Search Optimization For Motor Imaging EEG Feature Selection" Clinical EEG And Neuroscience https://Doi.Org/10.1177/15500594251325273 ISSN: 1550-0594 Online ISSN: 2169-5202 ESCI Journal Q2 Journal (Scopus And WOS Indexed) 2. Madumidha, S. ; Simhadati, Prasanna ; Soujanya, K.; **Karunakaran, S**. ; Kanagaraju, P. ; Sarode, Ghanasham C. ; Bhoopathy, V. ; Kavitha, N. S Quantum Dot-Driven Sensors For Precision Agriculture: Enhancing Crop Yield Predictions Through AI And Nanotechnology Journal: Journal Of Environmental Protection And Ecology 26(1) (2025) Pages: 287 – 300 , (Scopus Indexed) 3.M.Karthikeyan, Srinivasarao Thota, K.Sailaja Kunar, Dr Umanesan R, **S. Karunakaran**, Manne Renuka"Optimizing Financial Security With Cloud AI: Implementing Deep Q-Network and Transfer Learning For Risk Management And Fraud Detection" 2025 International Conference on Emerging Smart Computing And Informatics (ESCI) AISSMS Institute of Information Technology, Pune, India. Mar 5-7, 2025 : IEEE Conference Doi: 10.1109/Esci63694.2025.10988191 : 09 May 2025 (Scopus Indexed) 4.Krishna Azithtejaganti, Venkata And Senthilkumar, K.P. and Robinson L, Thomas and **Karunakaran, S**. And Pandugula, Chandrashekar and Khatana, Kavita, Energy-Efficient Real-Time Hybrid Deep Learning Framework For Adaptive IOT Intrusion Detection With Scalable and Dynamic Threat Mitigation (November 15, 2024). Proceedings Of The 3rd International Conference On Optimization Techniques In the Field of Engineering (ICOFE-2024), http://Dx.Doi.Org/10.2139/Ssrn.5077540 : Elsievier Publications: Indexing Date : 6 Jan 2025 (Scopus indexed) 5.P.Nageswara Rao, **S.Karunakaran**,Rachakonda Satish and Bukka Uday Kiran "2X2 MIMO Antenna with increased isolation" EAI International Conference on Intelligent systems with Applications in Communications, Computing and IoT (ICISCCI 2024) P.no: 151-158 ,18th July 2025 ,Springer Publications (Scopus Indexed)		

	6.**S. Karunakaran** ,S. Srivardhan ,M.Harshith ,and K. SaiManish "Low Power VLSI Architecture for Rail To Rail Dynamic Voltage Comparator" ICST Institute for Computer Sciences, Social Informatics and Telecommunications Engineering 2025 Published by Springer Nature Switzerland AG 2025. BROADNETS 2024, LNICST 601, pp. 114–121, 2025. : https://doi.org/10.1007/978-3-031-81168-5_11 (Scopus INDEXED) 7. K.S.Balamurugan, Jyoti Dhanke, **S.Karunakaran**, Manka Manwal and J.Samson Isaac "An innovative Real time Medical Devices and Sensors cardiac monitoring Applications using NI myRIO-1900 and IoT Cloud" Technological Applications for Smart Sensors : Intelligent Applications for Real-Time Strategies Published by : CRC Press (Taylor & Francis Group) Apple Academic Press (AAP) Indexing : (Scopus and Web of Science) 8. **S. Karunakaran** ,S. Srivardhan ,M.Harshith ,and K. Sai Manish "Low Power VLSI Architecture For Variable Gain Amplifier Using Pseudo Current Steering Gain Tuning Method" (WCONF) 2024 10.1109/WCONF61366.2024.10692229 : IEEE Conference :Indexing Date:04 October 2024 (Scopus Indexed) 9. **S.Karunakaran** , N. Nikhilesh; V. Nithesh; Kaustubh Singh "Implementation of Level Shifters Using Logic Error Detection" AMATHE 2024 : Date of Indexing : 12 July 2024: 10.1109/AMATHE61652.2024.10582126 IEEE Conference (Scopus Indexed) 10. **S.Karunakaran** , "High Performance VLSI Architecture of FIR filter for Seismic signal processing", 2023 IEEE Sponsored Third International Conference on Advances in Electrical, Computing, Communications and Sustainable Technologies (ICAECT 2023) , Shri Shankaracharya Technical Campus (SSTC), Bhilai, Chhattisgarh, India during 05 - 06, January 2023. (IEEE Conference) Electronic ISBN:978-1-6654-9400-7 DOI: 10.1109/ICAECT57570.2023.10118035 (IEEE Conference Scopus Indexed) 11. **S. Karunakaran**, T.Sai Kiran N.Lokesh Reddy,E.Swapna "Low Power and High speed Two stage Comparator" 2023 IEEE Sponsored Third International Conference on Advances in Electrical, Computing, Communications and Sustainable Technologies (ICAECT 2023) , Shri Shankaracharya Technical Campus (SSTC), Bhilai, Chhattisgarh, India during 05 - 06, January 2023. Electronic ISBN:978-1-6654-9400-7 DOI: 10.1109/ICAECT57570.2023.10117941 (IEEE Conference Scopus Indexed) 12. R. Yamini, **S.Karunakaran**, Sunil Kumar RM, Prathiba.L, Narender Chinthamu, Lakshmi B N, P Kiran Kumar "Improved Network Framework for Cloud Manufacturing Through Blockchain Technology" European Chemical Bulletin 2023, 12(Special Issue 3), 627-634, 2023. (ISSN 2063 5346) Month and year : 15th March 2023 https: DOI: 10.31838/ecb/2023.12.s3.072 13. M.Guru Vimal Kumar, **S.Karunakaran**, Shanker Chandre, Rakesh Kumar Godi, Manirajkumar P, Allam Balaram "Recognition and Implementation of Microgrid Digital Twin System For Unmanned Vehicles with Cloud Computing Techniques" Journal : SN Computer Science Volume 4 Issue 5 29th July 2023 ISSN:2662-995XE-ISSN:2661-8907 Publisher:Springer Nature (Scopus Indexed)

	14.**S.Karunakaran**, J.Vamshi Krishna , Abhinav Reddy, VLSI Implementation of a Energy Recovery 4:2 Compressor using PBL in International Conference on Artificial Intelligence Trends and Pattern Recognition organized by Vardhaman College of Engineering, Hyderabad held during 10-12 th March 2022 (IEEE Conference Scopus Indexed) 15. Devesh Pratap Singh, Susheel George Joseph, V. Tamil Selvi, **S. Karunakaran** , Appasami G.; B. Jegajothi "Quasi-Oppositional Satin Bowerbird with Deep Learning based Content based Image Retrieval"ICCMC,13th April ,2022 DOI: 10.1109/ICCMC53470.2022.9754135 (IEEE Conference SCOPUS Indexed) 16. **S.Karunakaran**, Jeevan Kumar, B. Aditya "VLSI Implementation of a High Speed Multiplier Using on the Fly Conversion Technique" "ECS Transactions" (ECST) from the First International Conference on Technologies for Smart Green Connected Society 2021 (IEEE Conference SCOPUS Indexed) 17. **S.Karunakaran** , VLSI Implementation of low Power Thermometer code to Digital converter using Wallace tree encoder International Conference on Power control and computing technologies (ICPC2T), NIT, Raipur , 1-3 March 2022 (IEEE Conference SCOPUS Indexed) 18. **S. Karunakaran**, K Pavan, P Rahul Reddy "VLSI Implementation of a High Speed and Area Efficient N-bit Digital CMOS Comparator" 2nd International Conference on Smart Technologies in Computing, Electrical and Electronics 16th and 17th December 2021 Reva University , Bengaluru DOI: 10.1109/ICSTCEE54422.2021.9708574 (IEEE Conference SCOPUS Indexed) 19. **S.Karunakaran**, Snehith. P "High Performance VLSI Architecture of Multiplexer and Demultiplexer Using various Adiabatic Logic" 2nd International Conference on Smart Technologies in Computing, Electrical and Electronics 16th and 17th December 2021 Reva University , Bengaluru DOI: 10.1109/ICSTCEE54422.2021.9708556 (IEEE Conference SCOPUS Indexed) 20. J RamaDevi; S Pathur Nisha; **S.Karunakaran**; S Hemavathi; Sankararao Majji; Anandaraj Shunmugam "Machine Learning Techniques for the Energy and Performance Improvement in Network –On- Chip", 2021 4th International Conference on Computing and Communications Technologies (ICCCT) 16-17 Dec.2021 DOI: 10.1109/ICCCT53315.2021.9711872 (IEEE Conference SCOPUS Indexed) 21. Veerraju G, Praful Vijay Nandankar, M. Kathiravan, **S. Karunakaran**, Arun Reddy Nalla, Ranjith Reddy Gaddam "Early prediction and analysis of corona pandemic outbreak using deep learning technique" World Journal of Engineering ISSN: 1708-5284 14th July 2021 https://doi.org/10.1108/WJE-03-2021-0145 (SCOPUS Indexed) 22.Akshaya M,Harshitha R, Sanjana M. **Karunakaran S** "High-Performance MUX And 6-T XOR Based 5-2 And 7-2 Compressors for Enormous Partial Products Computations" International Conference on Advances in Signal Processing, VLSI, Communications and Embedded Systems(ICSVCE 2022) , AIP Conference Proceedings (29 & 30 July 2022) (SCOPUS Indexed)

	23. **S.Karunakaran** , P. Tamilarasu, M.Sugumaran, P.N.Palanisamy , "Low Power VLSI design of TSPC D Flipflop" Jour of Adv Research in Dynamical & Control Systems, Vol. 12 | 08-Special Issue 2020 24.**S.Karunakaran**, T.Logeswaran,S.Shruti, R.Shravya, Thota Kavya, Performance Analysis of ALU design using irreversible and Reversible gates ," Jour of Adv Research in Dynamical & Control Systems, Vol. 12 | 08-Special Issue 2020 25. S.Arockiaraj , **S.Karunakaran** , P.Tamilarasu "Mitigation and analysis of sub synchronous resonance for DFIG based wind farm using STATCOM controller" IOP Conf. Series: Materials Science and Engineering 1055 (2021) 012140 doi:10.1088/1757-899X/1055/1/012140 26. M. Narayana, P.Tamilarasu, **S.Karunakaran**, Ch.Subrahmanyam "A Scale and Rotation Invariant Fast Image Mining For Shapes" IOP Conf. Series: Materials Science and Engineering 1055 (2021) 012097 doi:10.1088/1757-899X/1055/1/012097 27.**S.Karunakaran**, B.Poonguzharselvi "High Performance VLSI Architecture for Braun Multiplier" International Journal of Innovative Technology and Exploring Engineering (IJITEE) , Volume-8 Issue-10, August 2019 (Scopus Indexed) 28. **S.Karunakaran** and B.Poonguzharselvi "Investigations on power dissipation of low power VLSI architectures for Voltage level shifters" Jour of Adv Research in Dynamical & Control Systems, Vol. 11, Special Issue-05, 2019 (Scopus Indexed) 29. **S.Karunakaran** and Naveen Kishore Gattim" VLSI Implementation of Folded FIR filters using High Speed Multipliers" Journal of Engineering and Applied Sciences Vol 14 issue 4 ; pp 1070- 1077, ,2019. (SCOPUS Indexed) 30. K. Jaiganesh, P. Arulkumar, **S.Karunakaran**, Md. Asif, N. Srinivas "Improving the Efficiency of Solar Photovoltaic Cell by Decreasing Surface Temperature" International Journal of Engineering and Advanced Technology (IJEAT) , Volume-9 Issue-2, December, 2019 31. Fatima Unnisa, K.Jaiganesh, P.Arulkumar, **S.Karunakaran** "Direct Coupled PV Panel with ĆUK Converter for DC Load Applications" International Journal of Innovative Technology and Exploring Engineering (IJITEE) , Volume-9 Issue-2, December 2019. 32. **S.Karunakaran**, B.Poonguzharselvi,M.Narayana "Analysis of Low Power VLSI Design of Adder Cells" Jour of Adv Research in Dynamical & Control Systems, Vol. 10, 14-Special Issue, 2018(Scopus Indexed) 33. **S.Karunakaran** , Boddupally Harshitha , B.Poonguzharselvi , K.Jai Ganesh "Exploration of power delay product [PDP] on feedback based dual edge triggered flip flop utilizing dual sleep and dual slack approach" International Journal of Engineering & Technology, 7 (4) (2018) 3388-3391 (Scopus Indexed) 34.**S.Karunakaran**, Y.Pandurangaiah, Joseph Anthony Prathap, B.Poonguzharselvi "Exploration on Power Delay Product of Various VLSI Multiplier Architectures" International Journal of Mechanical Engineering and Technology(IJMET), Volume 9, Issue 1, January 2018, pp. 53–59 (Scopus Indexed)

	35. **S.Karunakaran**, N K Gattim "Multimodal Image fusion using curvelet and genetic algorithm" Journal of Scientific and Industrial Research, Vol 78, Nov 2017, pp 694-696 (Scopus Indexed) 36. **S.Karunakaran** "Exploration on power delay product of basic logic gates for various CMOS logic styles", International Journal of Engineering Studies. Volume 9, Number 2 (2017), pp. 111-120. (Scopus Indexed) 37. **S.Karunakaran**,"VLSI Architecture of an 8 bit multiplier using Vedic Mathematics in 180 nM technology", International Journal of Advances in Engineering & Technology ,June 2017 . 38. **S.Karunakaran** "Investigations on the performance of the basic logic gates for various CMOS logic structures", National conference on Emerging trends in Electronics and Computer Applications, Oct 20-21,2016 at Srinidhi Institute of Science and technology, Hyderabad. 39. **S.Karunakaran**, Rukmanidevi, S 2015,'Low latency and less power dissipation of a 4:2 compressor based distributed arithmetic unit FIR filter design', International Journal of Applied Engineering Research, vol. 10,no. 9 pp. 23465-23477. (Scopus Indexed) 40. **S.Karunakaran**, Kasthuri, N 2012, 'VLSI Implementation of FIR Filter Using Computational Sharing Multiplier Based On High Speed Carry Select Adder", American Journal of Applied Sciences, vol. 9, no. 12, pp. 2028-2045. (Scopus Indexed) 41. **S.Karunakaran**, Kasthuri, N 2012, 'High Performance VLSI Architecture for FIR filter Using On- the-Fly Conversion Multiplier', European Journal of Scientific Research, vol. 67, no. 4, pp.625- 635. (Scopus Indexed) 42. **S.Karunakaran**, Kasthuri, N 2011, 'Area and Power Efficient VLSI Architecture for FIR filter using Asynchronous Multiplier', British Journal of Science, December, vol. 2, no. 2, pp. 61-77. 43. **S.Karunakaran**, Gowrisankar ,V 'High speed VLSI Architecture for distributed Arithmetic FIR filter using compressors' International conference on CSCT presented on 5th May 2010 at Einstein college of Engineering ,Tirunelveli 44. **S.Karunakaran**, Murugesan,G, Premkumar,P, "Design of Power Efficient Folded FIR Filter Structures using Modified Booth Recoding Multiplier" International Conference on CSCT presented on 8th May 2010 at Cape Institute of Technology,Tirunelveli. 45.**S.Karunakaran**, Nidhin Joe Kuttikat "VLSI Implementation of Adaptive FIR filter using distributed arithmetic" National Conference on CI presented on 4th April 2009. 46. **S.Karunakaran**, Arun C., Muthukumaran S. and Rajamani V., 'Low Power VLSI Architecture for Viterbi Decoder', 2nd National Conference on TICAE-07, Presented on 15th -17th March 2007, Sathyabama University, Chennai.

<table>
<tr><td>Papers Presented in Conferences
(Scopus / WoS indexed only)</td><td>Overall : 21</td><td>After Joining RMK: -</td></tr>
<tr><td>Ph.Ds / Projects Guided</td><td>Ph.Ds Guided : -</td><td>Students Projects Guided: 55</td></tr>
<tr><td>Books Published :</td><td colspan="2">Count: 4</td></tr>
<tr><td></td><td colspan="2">List:
1. Prof.Ravi Mohan, Dr.S.Karunakaran, Dr.Manthan S.Manavadaria, Dr.J.Muralidharan : “A Text Book of VLSI”,2023, RK Publications (ISBN :978-81-19140-04-06)

2. Dr.M.prasad, Dr.S.Karunakaran, Dr.R.Priscilla “A modern GPU ZEN/ A modern Graphical Processing Unit ZEN” 2024,PKS Publication : ISBN : 978-81-964693-0-6

3. Dr.Anand Deva Durai C, Dr.S.Karunakaran,Dr.Priya Velayutham, G.Deepa “ A Textbook of Deep Learning” ,2024,RK Publications ISBN : 978-81-971649-8-9

4. Sri Suryakanta, Dr.S.Karunakaran , Dr.Nitin , Dr.Pratibha “Nanoscience and Nanotechnology” , BR Publications, 2025 ISBN : 978-93-47231-18-6</td></tr>
<tr><td rowspan="2">Patents</td><td>Published Count: 4</td><td>Granted Count: 3</td></tr>
<tr><td colspan="2">List:
1. Single Electron Transistor Intelligent logic for High Reliability of Moore's low power Advanced VLSI (Patent number: 202141059650) (Indian Patent) Status : (Granted)

2. Next Generation Framework for Smart building monitoring using 6LoWPAN (Patent number: 2020102608), Australian Patent (Granted)

3. Aerial Manipulative Omni Directional Drones for Building Construction (Patent number: 2020102606) , Australian Patent. (Granted)

4. Advanced VLSI-chip design and Production Process Patent number :202241052157 Filing date :13/09/2022 Publication Date : 23/09/2022 (Indian Patent) Status : Published

5. Improved Cyber Security using Machine Learning (Patent number 202241052150) Filing date : 13/09/2022 Publication Date : 23/09/2022 (Indian Patent) Status : Published

6. Interface the two VLSI chip using AI : (Patent number 202541039242) Filing date : 23/04/2025 Publication Date : 16/05/2025 (Indian Patent) Status : Published</td></tr>
</table>

	7. To transform the VLSI on the Virtual Mode (e-VLSI) with AI Driven 6G systems: (Patent Number 202541037984) Filing date : 21/04/2025 Publication Date : 16/05/2025 (Indian Patent) Status : **Published**
Professional Memberships	Count : 3
	➢ Life Member -ISTE (LM 59445) ➢ IEEE Member (97242270) ➢ IEEE Council of Electronics Design Automation Tools
Consultancy Projects Completed	Count : - --
Awards Received	Count : 1
	"Academic Excellence award 2021 for Excellent Researcher" on the occasion of International Conference & Academic Excellence Award On Recent Innovation and Interdisciplinary Research 2021 organized by International Association of Research and Developed Organization in association of All India Council for Productive Education, affiliated to Vigyan Prasar ,DST, Govt of India.
Research grants Received	Non-Inverting Buck-Boost Converter Design using Analog Multiplier, Vardhaman Research Promotion Scheme Project (VRPS) Duration : 6 months : Rs 40,000/-
Orchid Link / ID	https://orcid.org/0000-0002-3584-7119
Google Scholar Link / ID	https://scholar.google.com/citations?user=L6ZSoC4AAAAJ&hl=en&authuser=1
Vidwan Link / ID	https://vidwan.inflibnet.ac.in/myprofile/241948
Research Gate Link / ID	https://www.researchgate.net/profile/Karunakaran?ev=prf_overview
Scopus Link / ID	https://www.scopus.com/authid/detail.uri?authorId=57199753158