DECLARATION BY THE CANDIDATE

The given information is true to the best of my knowledge. I agree to abide by the rules and regulations governing the programme. If selected, I shall attend the course for the entire duration. In case I am unable to attend the course, I am prepared to forego the refundable advance paid by me (if applicable).

Place :

Date : Signature of the candidate

SPONSORSHIP

Mr./ Ms./ Dr.....
is an employee of our Institution and is hereby sponsored. He/she will be permitted to attend the programme, if selected. He/She will abide by the rules and regulations of the host Institute.

Date: Seal Signature of the Sponsoring authority

The duly filled application forms along with DD should be sent to,

Dr.S.Ramasamy
Co-ordinator-FDP
Department of Electronics & Communication Engg.
RMK Engineering College,
RSM Nagar, Kavaraipettai – 601 206
Tiruvallur Dist
Tamilnadu
Email: srs.ece@rmkec.ac.in

IMPORTANT DATES

Last date for receipt of applications	:	10-06-2013
Date of intimation regarding selection	:	11-06-2013
Confirmation by participants	:	12-06-2013

The selected candidates will be intimated only through e-mail. If required, kindly take photocopy of the registration form for multiple use.

ABOUT THE COLLEGE

Since its inception in 1995, R.M.K Engineering College has grown into a unique institution providing high quality academic environment. The college maintains close interaction with several R&D institutions. The National Board of Accreditation of AICTE has accredited seven programmes of the college.

The college is affiliated to Anna University and is certified under ISO 9001-2008. Presently, the college offers 7 under-graduate programmes and 7 post-graduate programmes. The college has well-equipped laboratories in all branches of engineering and also has close interactions with the Industries. The institution has excellent infrastructural facilities to support both undergraduate, postgraduate programmes and research activities. Currently,more than 100 Ph.D scholars are pursuing their research programmes

The College, located at a distance of about 35 km from Chennai on the Chennai - Vijayawada National Highway (NH 5), is easily reachable both by road and rail.

ABOUT THE DEPARTMENT

Electronics & Communication Engineering Department was started in the year 1995 and is accredited by NBA, AICTE. It has a team of well qualified, experienced and dedicated faculty members with research and teaching backgrounds. The laboratories are well equipped with modern training facilities that cater to the requirements of the university syllabus as well as the requirements of the industry. The department has attracted many significant research grants from AICTE, DST. The department has installed the state of the art **VLSI Lab** through non- revenue fund generation from **AICTE** under the scheme of **MODROBS and from the management funds.**The department offers two Post Graduate Courses in **VLSI Design and Applied Electronics. The department is recognized by the Anna University . To conduct Ph.D programs.**

AICTE FACULTY DEVELOPMENT PROGRAMME
ON

"HANDS ON TRAINING ON DESIGN FINISHING FOR CHIP TAPEOUT"

17-06-2013 TO 29-06-2013

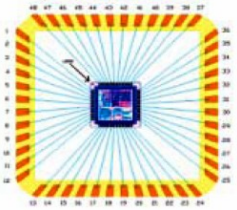
Sponsored by
ALL INDIA COUNCIL FOR TECHNICAL EDUCATION

Coordinator
Dr. S. Ramasamy

Organized by
Department of Electronics and Communication Engineering

R.M.K. Engineering College

R.S.M. NAGAR, KAVARAIPETTAI- 601 206.
GUMMIDIPOONDI TALUK, THIRUVALLUR DIST.
TAMIL NADU, INDIA
Phone : 044-27925102/338/339
http:// www.rmkec.ac.in



PREAMBLE

The trends in VLSI technology allow the complex systems of yesteryears to be fabricated as Systems on Chip. With the top 25 semiconductor companies present in India, the eco system is gradually moving toward product/design innovation. Since we do not have world class clean room/fab facilities, most the semiconductor industry in India is fabless company like Cosmic circuits, Innovative Logic India,Apsconnect, Techvulcan etc. With the Indian Government focusing on improving access to higher education and skilled manpower development on VLSI, it is responsibility of technical institution to supply talent work force to fabless semiconductor companies. In view of this, the staff development programme focus on imparting the complete knowledge on taping out a chip with the state of the art CMOS technology nodes.

OBJECTIVE

- To provide hands on training on System on Chip design
- To impart semiconductor design training to graduate engineers to make them industry ready
- To make use of open source EDA tools
- To expose the participants to industry sign off EDA tools
- To promote IP creation
- To use latest CMOS technology in class room teaching

COURSE CONTENTS

- Introduction to VLSI system design
- CMOS Technology
- VHDL/Verilog
- Digital, Analog and Mixed signal VLSI Design
- VLSI Verifications
- FPGA based System Design
- Linux for handling EDA tools
- Hands on with Open source EDA tools (Alliance)
- Lab session on Verification (ncsim, Modelsim, VCS)
- Lab session with synthesis (RTL compiler, Design vision)
- Lab session with PAR tools (SoC encounter)
- Lab session with Static Timing Analysis
- Lab session with Analog Design (Spectre & Virtuoso)
- Lab session with Physical versification (Assura, Calibre)
- Full chip integration
- Board issues & testing the chip

COURSE FACULTY

Faculty from premier Institutions like IIT, NIT, experts from Semiconductor companies and R&D organizations.

ELIGIBILITY

The course is open to the engineering teachers of wired disciplines who are working in Engineering Colleges/Polytechnics. Teachers belonging to other disciplines may also apply if this course would supplement their research. Admission will be offered subject to the availability based on the AICTE guidelines.

ACCOMMODATION

Accommodation will be provided to the outstation participants, on request.

PARTICIPANTS FROM OTHER ORGANISATIONS

Engineers working in R&D Organizations/Industries are also eligible to apply. A course fee of Rs. 10,000/- (for industry Participants only) should be sent by Cheque/DD drawn in favour of "**The Principal, RMK Engineering College,** payable at chennai.

REGISTRATION

The registration is free for **faculties from AICTE approved Institutions.** Selected participants are requested to pay an amount of Rs. 500/- by DD drawn in favour of **"The Principal, RMK Engineering College,** payable at **Chennai** which is refundable after the successful completion of the programme.

REGISTRATION FORM

AICTE Sponsored

FACULTY DEVELOPMENT PROGRAMME

ON

"HANDS ON TRAINING ON DESIGN FINISHING FOR CHIP TAPEOUT"

17th to 29th June, 2013

Name: Dr./Mr./Ms:----------

Academic Qualification: ----------

Designation/Dept.:----------

Years of teaching experience: ----------

Phone/Fax: ----------

E-mail:----------

Address: ----------

PIN code: ----------

Is the institution approved by AICTE? Yes/No

Do you want accommodation? Yes/No

DD No: ---------- Date: ----------

Bank: ----------Place: ----------

Signature of the Applicant